## ZXFV302

## 4:1 HIGH SPEED MULTIPLEXER

## DEVICE DESCRIPTION

The ZXFV302 is a $4: 1$ high speed analog switch designed for use as a buffered video multiplexer and other high-speed applications.

It features low different gain and phase distortion. The high speed high output current capability provides $75 \Omega$ cable drive for use in high performance video applications.

The input channel is selected by means of two logic lines using an internal decoder. An output enable line allows expansion to eight channels using two devices ZXFV302 as shown in the example application figure 1.

An alternative device, ZXFV301 provides the same functionality and pin-out as the ZXFV302 but with four separate logic lines controlling the switch channels directly.

## Connection Diagram



## Ordering information

| Part Number | Container | Increment |
| :---: | :---: | :---: |
| ZXFV302N16TA | Reel 7" | 500 |
| ZXFV302N16TC | Reel 13" | 2500 |

## FEATURES AND BENEFTTS

- 3dB Bandwidth 300M Hz
- Slew rate 450V/ $\mu \mathrm{s}$
- Differential gain 0.01\%
- Differential phase $0.04^{\circ}$
- Output current 40mA
- Stable up to 100pF load
- $\pm 5$ Volt supply
- Supply current 17mA
- 16 pin SO package


## APPLICATIONS

- Video routing and switching
- CCTV switching
- Video distribution selection
- RGB multiplexing
- High frequency instrumentation Data acquisition
- Data acquisition


Fig.1:Typical Application for 8 channel CCTV

## ZXFV302

## ABSOLUTE MAXIMUM RATINGS

Supply voltage VCC
Supply voltage VEE
Analog inputs to ground
Digital inputs to ground
Outputs to ground*
Output current, max continous
Operating Ambient Temperature Range Operating J unction temperature $\mathrm{T}_{\mathrm{J}}$ MAX
-0.5 V to +6 V
-6 V to +0.5 V
$\mathrm{V}_{\mathrm{EE}}-0.5 \mathrm{~V}$ to V CC +0.5 V
-0.5 V to V cc +0.5 V
Vee -0.5 V to VCC +0.5 V
40 mA
$-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ Storage $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$
$150^{\circ} \mathrm{C}^{* *}$
**The thermal resistance from the semiconductor die to ambient is typically $120^{\circ} \mathrm{C} / \mathrm{W}$ when the SO 16 package is mounted on a PCB in free air. The power dissipation of the device when loaded must be designed to keep the device junction temperature below $\mathrm{T}_{\mathrm{J}}$ MAX.
*During power-up and power-down, these voltage ratings require an appropriate sequence of applying and removing signals and power supplies.

## ELECTRICAL CHARACTERISTICS

$\pm 5 \mathrm{~V}$ power supplies, $\mathrm{T}_{\text {amb }}=25^{\circ} \mathrm{C}$ unless otherwise stated. $\mathrm{R}_{4}=150 \Omega, \mathrm{C}_{1}=10 \mathrm{pF}$
Characteristics apply to channel selected, and EN input HIGH unless otherwise stated
Test level: $\quad P=100 \%$ production test
C = characterised only

| PARAMETER | CONDITIONS | TEST | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage V+ |  |  | 4.75 | 5 | 5.25 | V |
| Supply Voltage V- |  |  | -5.25 | -5 | -4.75 | V |
| Positive supply current |  | P | 13 | 17 | 21 | mA |
| Negative supply current |  | P | 9 | 13 | 18 | mA |
| Voltage gain DC |  | P | 0.99 | 1.000 | 1.01 | VN |
| Input Common mode Voltage |  | P |  | $\pm 3$ |  | V |
| Input resistance |  | P |  | 45 |  | k $\Omega$ |
| Output offset Voltage | All channels held at 0V | P | -10 | +11 | +30 | mV |
| Input bias current | Active channels held at OV | P | -25 | -11 | +5 | $\mu \mathrm{A}$ |
| Output Voltage swing |  | P |  | $\pm 3$ |  | V |
| Output drive current |  | P | 40 |  |  | mA |
| Output resistance |  | C |  |  | 1 | $\Omega$ |
| Output resistance | Disabled (EN Iow) | P | 1.5 | 3 | 4.5 | M $\Omega$ |
| Positive PSRR |  | P | 40 | 54 |  | dB |
| Negative PSRR |  | P | 30 | 51 |  | dB |
| Small signal bandwidth ${ }^{1}$ |  | C |  | 300 |  | MHz |
| Slew rate, 25\% to 75\% | 2V pk-pk | C |  | 450 |  | V/us |
| Logic input HIGH $\mathrm{V}_{\text {Hmin }}$ |  | C |  |  | 2 | V |
| Logic input LOW $\mathrm{V}_{\text {Lmax }}$ |  | C | 0.8 |  |  | V |
| Logic input current $\mathrm{I}_{\text {INHIGH }}$ | logic input voltage $=5 \mathrm{~V}$ | C |  | 5 |  | pA |
| Logic input current $\mathrm{I}_{\text {INLOW }}$ | logic input voltage $=0 \mathrm{~V}$ | C |  | -70 |  | $\mu \mathrm{A}$ |

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## ELECTRICAL CHARACTERISTICS

$\pm 5 \mathrm{~V}$ power supplies, $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$ unless otherwise stated. $\mathrm{R}_{\mathrm{L}}=150 \Omega, \mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ Characteristics apply to channel selected, and EN input HIGH unless otherwise stated

Test level: $\mathrm{P}=100 \%$ production test
C = characterised only

| PARAMETER | CONDITIONS | TEST | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{ON}}$ | Vout $= \pm 2 \mathrm{~V}$, see timing diagram | C |  | 35 |  | ns |
| toff | Vout $= \pm 2 \mathrm{~V}$, see timing diagram | C |  | 10 |  | ns |
| t LOW | Vout $= \pm 2 \mathrm{~V}$, see timing diagram | C |  | 50 |  | ns |
| $\mathrm{t}_{\text {HIGH }}$ | Vout $= \pm 2 \mathrm{~V}$, see timing diagram | C |  | 40 |  | ns |
| Cross-talk, all hostile ${ }^{1}$ | $10 \mathrm{MHz}, 0 \mathrm{dBm}$ in | C |  | 75 |  | dB |
| Differential Gain |  | C |  | 0.01 |  | \% |
| Differential Phase |  | C |  | 0.04 |  | deg |
| Switching transients, magnitude | All channels held at 0V | C |  | 50 |  | mV |
| Switching transients, duration | All channels held at 0V | C |  | 25 |  | ns |

Notes:

1. Bandwidth and cross talk measured using Zetex Evaluation Circuit Board detailed later in this datasheet.

Truth table for selection of input channel

| A1 | A0 | EN | OUT |
| :---: | :---: | :---: | :---: |
| $X$ | $X$ | 0 | Hi $Z$ |
| 0 | 0 | 1 | IN 1 |
| 0 | 1 | 1 | IN 2 |
| 1 | 0 | 1 | IN 3 |
| 1 | 1 | 1 | IN 4 |

Fig.2: TIMING DIAGRAM


Notes: The 'select' waveform represents a change in the the 2 bit control word A0 and A1.
$\mathrm{t}_{\text {HIGH }}$ is equivalent to $\mathrm{t}_{\text {Low }}$ but, applies for a positive going transition of OUT.

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## CHARACTERISTICS



## APPLICATIONS INFORMATION

## Introduction

A typical circuit application is outlined in Figure 1, above, where two devices are combined to provide 8-to-1 multiplexing. A more detailed basic application circuit for 4 dc-coupled channels is given in Figure 3, and an AC coupled circuit for 8 channels is shown in Figure 4. These circuits are suitable for $75 \Omega$ transmission line connections at both the input and the output and are useful for distribution of wide-band signals such as video via cables. The $75 \Omega$ reverse terminating resistor at the output gives the correct matching condition to a terminated video cable. The amplifier load is then $150 \Omega$.

The wide bandwidth of this device necessitates some care in the layout of the printed circuit. Partly for this reason, an Evaluation Circuit board is available and is described in a later paragraph. A continuous ground plane is required under the device and its signal connection paths, to provide the shortest possible ground return paths for signals and power supply filtering. A double-sided or multi-layer PCB construction is required, with plated-through via holes providing closely spaced low-inductance connections from some components to the continuous ground plane (some of these holes are not visible in the figures for the Evaluation Circuit Board - artworks and NC drill output can be provided if required).

For the power supply filtering, low inductance surface mount capacitors are normally required. It has been found that very good RF decoupling is provided on each supply using a 1000 pF NPO size 0805 ceramic surface mount capacitor, closest to the device pin, with an adjacent $0.1 \mu \mathrm{~F}$ X7R capacitor. Other configurations are possible and it may be found that a single $0.01 \mu \mathrm{~F}$ or $0.1 \mu \mathrm{~F}$ X7R capacitor, size 0805 or smaller, on each supply gives good results. However this should be supported by larger decoupling capacitors elsewhere on the printed circuit board. Values of 1 to $10 \mu \mathrm{~F}$ are recommended, particularly where the voltage regulators are located more than a few inches from the device. These larger capacitors are recommended to be solid tantalum electrolytic or ceramic types.

## Evaluation Circuit

An evaluation circuit is available, constructed on a double-side printed circuit board. The circuit is suitable for both the ZXFV301 and ZXFV302 and either device may befitted. Figures 5 and 6 show the circuit diagram, and the layout of components and copper. A parts list is provided below. This layout serves as a useful example for many applications, showing the practical implementation of the advice given above in the Introduction.

BNC connector sockets allow connection to test instruments via $50 \Omega$ cables. The output circuit includes a resistor matching circuit to present a load of $150 \Omega$ to the device and simultaneously provide $50 \Omega$ output impedance. The attenuation of this matching circuit is 15.45 dB . As the device has unity voltage gain, the overall loss when loaded by $75 \Omega$ is also 15.45 dB .

## EVALUATION CIRCUIT PARTS LIST:

| QTY | CCT-REF | VALUE | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| Resistors, surface mount |  |  |  |
| 4 | R1,R2,R3,R4 | 51R | 0805 |
| 4 | R5,R6,R7,R8 | 22k | 0805 |
| 1 | R9 | 120R | 0805 |
| 1 | R10 | 62R | 0805 |
| 1 | R11 | 10R | 0805 |
| 5 | R12 to R16 | 47k | 0805 |
| Capacitors, surface mount |  |  |  |
| 6 |  | 100nF | $\begin{aligned} & \text { 25V ceramic } 0805 \\ & \text { X7R } \end{aligned}$ |
| 2 |  | 1nF | 50V ceramic 0805 NPO |
| 2 |  | 10رF | $\begin{aligned} & \text { 16V Tant Elec size } \\ & \text { C } \end{aligned}$ |
| Integrated Circuits |  |  |  |
| 1 | U1 | - | Zetex ZXF 301N16 or ZXFV302N16 |
| Miscellaneous |  |  |  |
| 5 |  | - | BNC Socket, PCB straight flange, e.g. Tyco B35N 14H999X99 |
| 1 |  | - | 3-way PCB screw terminal block IMO 20.501/3SB |
| 1 | SW1 | - | DIL switch, 8 way |
| 10 | TP1 to TP10 | - | PCB test terminal, red, W.Hughes 100-107 |

SIGNAL INPUTS， $75 \Omega$

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## ZXFV302


$\underset{\text { JF, }}{\substack{* 1 E L D C K A G E=I M O 17 A 3 W}}$


Figure 5: EVALUATION CIRCUIT \& PRINTED BOARD LAYOUT SHOWING TOP COPPER (overall dimensions $4 \times 3$ inches)

ZXFV302


Figure 6: EVALUATION CIRCUT BOARD BOTTOM COPPER
(viewed through from top)

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Notes

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Notes

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PACKAGE OUTLINE


| DIM | Millimetres |  |  | Inches |  |
| :--- | :--- | :--- | :--- | :--- | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 9.80 | 10.00 | 0.386 | 0.394 |  |
| B | 1.27 BSC | 0.05 BSC |  |  |  |
| C | 0.53 REF | 0.02 REF |  |  |  |
| D | 0.33 | 0.51 | 0.013 | 0.020 |  |
| E | 3.80 | 4.00 | 0.15 | 0.157 |  |
| F | 1.35 | 1.75 | 0.053 | 0.069 |  |
| G | 0.10 | 0.25 | 0.004 | 0.01 |  |
| H | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |  |
| I | 0.40 | 1.27 | 0.016 | 0.05 |  |
| J | 5.80 | 6.20 | 0.228 | 0.244 |  |

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